EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	14248209	@ad<"19960822"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/01/07 23:13
L2	32393	"711"/$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/01/07 23:15
L3	726571	software	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/01/07 23:15
L4	542650	hardware	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/01/07 23:15
L5	301	DLAT	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/01/07 23:15
L6	331734	L3 and L4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/01/07 23:15
L7	5490	TLB	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/01/07 23:15
L8	61	L6 and L5	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/01/07 23:15
L9	1571562	target address	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/01/07 23:15

EAST Search History

L10	15	L8 and L7	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/01/07 23:15
L11	15	L10 and L9	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/01/07 23:15
L12	2684802	memory protection	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/01/07 23:15
L13	19156	prevent$4 near3 writ$4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/01/07 23:15
L14	13377	L12 and L13	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/01/07 23:15
L15	0	L11 and L14	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/01/07 23:15
L16	37	(kelly near edmund).in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/01/07 23:16
L17	20	(cmelik near robert).in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/01/07 23:16
L18	19	(wing near malcolm).in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/01/07 23:16
L19	49	L16 or L17 or L18	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/01/07 23:16

EAST Search History

L20	0	11 and 19	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/01/07 23:16

Terms used
prevent or **avoid** or **preempt** **sentence** **translation** **lookaside** **buffer** or **TLB** or **DLAT** **near/2** **target** **address** **se**

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Result page: **1** 2 3 4 5 6 7 8 9 10 ne

1 Cache Memories
Alan Jay Smith
September 1982 **ACM Computing Surveys (CSUR)**, Volume 14 Issue 3
Publisher: ACM Press
Full text available: pdf(4.61 MB) Additional Information: full citation, references, citings,

2 Mondrian memory protection
Emmett Witchel, Josh Cates, Krste Asanović
October 2002 **ACM SIGPLAN Notices , ACM SIGARCH Computer Architecture News , AC 10th international conference on Architectural support for programmin** Issue 10 , 5 , 5
Publisher: ACM Press
Full text available: pdf(1.53 MB) Additional Information: full citation, abstract, refe

Mondrian memory protection (MMP) is a fine-grained protection scheme that allows multiple pro services. In contrast to earlier page-based systems, MMP allows arbitrary permissions control at permissions table to reduce space overheads and employ two levels of permissions caching to re implementation add less than 9% overhead to ...

3 Energy efficient memory systems: Generating physical addresses directly for saving instru
I. Kadayif, A. Sivasubramaniam, M. Kandemir, G. Kandiraju, G. Chen
November 2002 **Proceedings of the 35th annual ACM/IEEE international symposium on I**
Publisher: IEEE Computer Society Press
Full text available: pdf(1.26 MB) Publisher Site Additional Information: full citation, abstract, refe

Power consumption and power density for the Translation Lookaside Buffer (TLB) are important cache design as well. This paper embarks on a new philosophy for reducing the number of acces optimizations. The overall idea is to keep a translation currently being used in a register and avc change. We propose f ...

4 Architectural support for translation table management in large address space machines
Jerry Huck, Jim Hays
May 1993 **ACM SIGARCH Computer Architecture News , Proceedings of the 20th a '93**, Volume 21 Issue 2

Publisher: ACM Press
Full text available: pdf(1.34 MB) Additional Information: full citation, abstract, refe

Virtual memory page translation tables provide mappings from virtual to physical addresses. Wh not contain a translation, these tables provide the translation. Approaches to the structure and r to complete software based algorithms. The size of the virtual address space used by processes

5 Exokernel: an operating system architecture for application-level resource management
D. R. Engler, M. F. Kaashoek, J. O'Toole
December 1995 **ACM SIGOPS Operating Systems Review , Proceedings of the fifteenth A**
Volume 29 Issue 5
Publisher: ACM Press
Full text available: pdf(2.16 MB) Additional Information: full citation, references, c

6 Software controlled memory systems: Energy-efficient address translation for virtual memc
Xiangrong Zhou, Peter Petrov
September 2005 **Proceedings of the 3rd IEEE/ACM/IFIP international conference on Har '05 , Proceedings of the 3rd IEEE/ACM/IFIP international conference or CODES+ISSS '05**
Publisher: ACM Press, IEEE Computer Society
Full text available: pdf(150.88 KB) Publisher Site Additional Information: full citation, abstract, refe

In this paper we present an application-driven address translation scheme for low-power and re power inefficiency and nondeterministic execution times of address-translation mechanisms hav memory in embedded processors with low-power and real-time constraints. To address this prol organization, where ...

Keywords: adaptable systems, multi-mode synthesis, reconfigurability

7 Mondrix: memory isolation for linux using mondriaan memory protection
Emmett Witchel, Junghwan Rhee, Krste Asanović
October 2005 **ACM SIGOPS Operating Systems Review , Proceedings of the twentieth**
Volume 39 Issue 5
Publisher: ACM Press
Full text available: pdf(332.09 KB) Additional Information: full citation, abstract, refe

This paper presents the design and an evaluation of Mondrix, a version of the Linux kernel with hardware and software that provides efficient fine-grained memory protection between multiple to enforce isolation between kernel modules which helps detect bugs, limits their damage, and i MMP exposed two kerne ...

Keywords: fine-grained memory protection

8 Recency-based TLB preloading
Ashley Saulsbury, Fredrik Dahlgren, Per Stenström
May 2000 **ACM SIGARCH Computer Architecture News , Proceedings of the 27th ai '00**, Volume 28 Issue 2
Publisher: ACM Press
Full text available: pdf(651.05 KB) Additional Information: full citation, abstract, refe

Caching and other latency tolerating techniques have been quite successful in maintaining high However, TLB misses have become a serious bottleneck as working sets are growing beyond the TLB miss latency by using preloading techniques. We present results for traditional next-page Tl

9 Disco: running commodity operating systems on scalable multiprocessors

Edouard Bugnion, Scott Devine, Kinshuk Govil, Mendel Rosenblum
November 1997 **ACM Transactions on Computer Systems (TOCS)**, Volume 15 Issue 4
Publisher: ACM Press
Full text available: pdf(400.76 KB) Additional Information: full citation, abstract, refe

In this article we examine the problem of extending modern operating systems to run efficiently implementation effort. Our approach brings back an idea popular in the 1970s: virtual machine operating systems on a scalable multiprocessor. This solution addresses many of the challenges approach with a prototy ...

Keywords: scalable multiprocessors, virtual machines

10 Hardware support for fast capability-based addressing

Nicholas P. Carter, Stephen W. Keckler, William J. Dally
November 1994 **ACM SIGPLAN Notices , ACM SIGOPS Operating Systems Review , Proce support for programming languages and operating systems ASPLOS-VI**,
Publisher: ACM Press
Full text available: pdf(1.07 MB) Additional Information: full citation, abstract, refe

Traditional methods of providing protection in memory systems do so at the cost of increased cc permissions for processes. With the advent of computers that supported cycle-by-cycle multithr context switch are unacceptable, but protecting unrelated processes from each other is still nece environments.This pap ...

11 Fast detection of communication patterns in distributed executions

Thomas Kunz, Michiel F. H. Seuren
November 1997 **Proceedings of the 1997 conference of the Centre for Advanced Studies**
Publisher: IBM Press
Full text available: pdf(4.21 MB) Additional Information: full citation, abstract, refe

Understanding distributed applications is a tedious and difficult task. Visualizations based on prc of the execution of the application. The visualization tool we use is Poet, an event tracer develo very complex and do not provide the user with the desired overview of the application. In our e: commun ...

12 Disco: running commodity operating systems on scalable multiprocessors

Edouard Bugnion, Scott Devine, Mendel Rosenblum
October 1997 **ACM SIGOPS Operating Systems Review , Proceedings of the sixteenth** Volume 31 Issue 5
Publisher: ACM Press
Full text available: pdf(2.30 MB) Additional Information: full citation, references,

13 Decoupled hardware support for distributed shared memory

Steven K. Reinhardt, Robert W. Pfile, David A. Wood
May 1996 **ACM SIGARCH Computer Architecture News , Proceedings of the 23rd a '96**, Volume 24 Issue 2
Publisher: ACM Press
Full text available: pdf(1.47 MB) Additional Information: full citation, abstract, refe

This paper investigates hardware support for fine-grain distributed shared memory (DSM) in net cost relative to dedicated DSM systems, we decouple the functional hardware components of DS two decoupled systems, Typhoon-0 and Typhoon-1. Typhoon-0 uses an off-the-shelf protocol pr

only DSM-specific hard ...

14 Shade: a fast instruction-set simulator for execution profiling

Bob Cmelik, David Keppel
May 1994 **ACM SIGMETRICS Performance Evaluation Review , Proceedings of the : modeling of computer systems SIGMETRICS '94**, Volume 22 Issue 1
Publisher: ACM Press
Full text available: pdf(1.28 MB) Additional Information: full citation, abstract, refe

Tracing tools are used widely to help analyze, design, and tune both hardware and software sys efficient instruction-set simulation with a flexible, extensible trace generation capability. Efficien and trace the application program. The user may control the extent of tracing in a variety of wa collected ...

15 Embedded systems: Arithmetic-based address translation for energy-efficient virtual mem

Xiangrong Zhou, Peter Petrov
September 2005 **Proceedings of the 18th annual symposium on Integrated circuits and s**
Publisher: ACM Press
Full text available: pdf(267.86 KB) Additional Information: full citation, abstract, refe

In this paper, we present an arithmetic-based address translation scheme for low-power and re purpose virtual memory support comes with its fundamental disadvantages of excessive power disadvantages have been the main reason for not adopting virtual memory and its associated be operations are major requirements. To ...

16 Virtual memory primitives for user programs

Andrew W. Appel, Kai Li
April 1991 **ACM SIGPLAN Notices , ACM SIGARCH Computer Architecture News , AC fourth international conference on Architectural support for programmi** 25 Issue 4 , 2 , Special Issue
Publisher: ACM Press
Full text available: pdf(1.37 MB) Additional Information: full citation, references,

17 The M-Machine multicomputer

Marco Fillo, Stephen W. Keckler, William J. Dally, Nicholas P. Carter, Andrew Chang, Yevgeny Gure
December 1995 **Proceedings of the 28th annual international symposium on Microarchitec**
Publisher: IEEE Computer Society Press
Full text available: pdf(1.29 MB) Additional Information: full citation, references, citings, inc

18 Multigrain shared memory

Donald Yeung, John Kubiatowicz, Anant Agarwal
May 2000 **ACM Transactions on Computer Systems (TOCS)**, Volume 18 Issue 2
Publisher: ACM Press
Full text available: pdf(369.18 KB) Additional Information: full citation, abstract, refe

Parallel workstations, each comprising tens of processors based on shared memory, promise co of such small- to medium-scale shared-memory multiprocessors through software over a local a these systems Distributed Shared-memory MultiProcessors (DSMPs). This article introduces the sharing, ca ...

Keywords: distributed memory, symmetric multiprocessors, system of systems

19 The interaction of architecture and operating system design

Thomas E. Anderson, Henry M. Levy, Brian N. Bershad, Edward D. Lazowska
April 1991 **ACM SIGPLAN Notices , ACM SIGARCH Computer Architecture News , AC fourth international conference on Architectural support for programmi** 25 Issue 4 , 2 , Special Issue

Publisher: ACM Press

Full text available: pdf(1.60 MB) Additional Information: full citation, references,

20 The effects of virtually addressed caches on virtual memory design and performance

Jon Inouye, Ravindranath Konuru, Jonathan Walpole, Bart Sears
October 1992 **ACM SIGOPS Operating Systems Review**, Volume 26 Issue 4

Publisher: ACM Press

Full text available: pdf(1.32 MB) Additional Information: full citation, abstract, ind

Recent times have witnessed rapid advances in microprocessor technology resulting in an order developments in hardware have been paralleled by several prominent trends in operating syster micro-kernels. However, operating system performance has not kept pace with that of the unde enhance processor performance can h ...

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